

A Timing Model for Synchronous Language Implementations in Simulink

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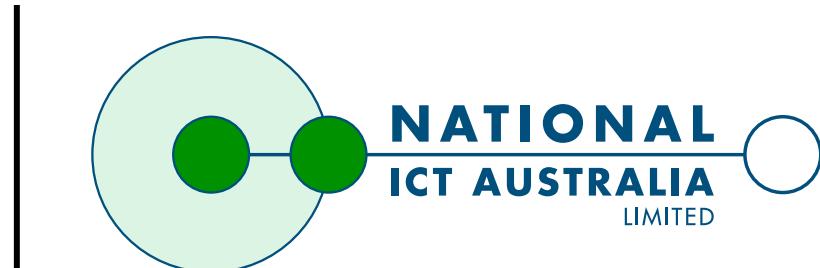
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Outline

⇒ Simulink and Stateflow

An Argos block

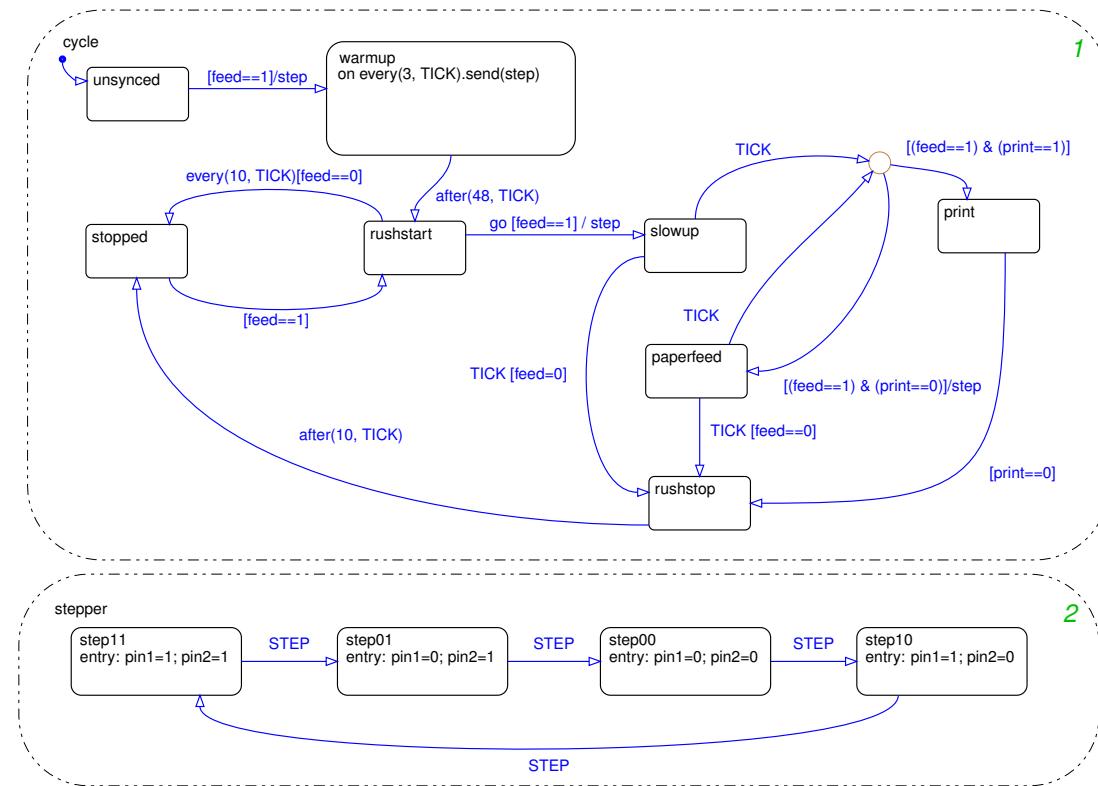
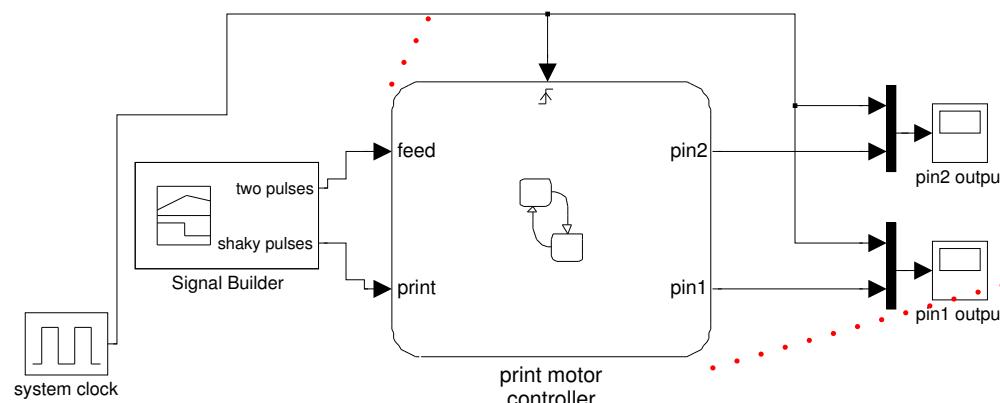
Timing Model

Embedding within Simulink

Concluding remarks

Simulink and Stateflow

- Popular tools
- Practical focus
- Several shortcomings



Simulation ↵ Model-driven Development

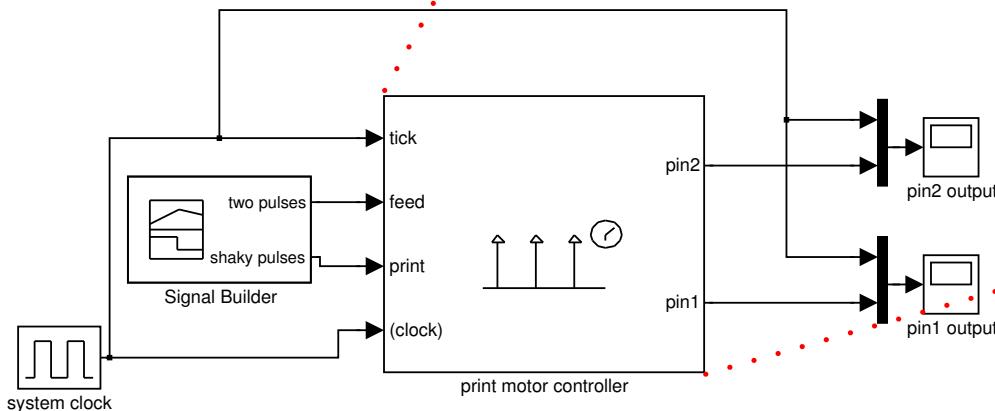
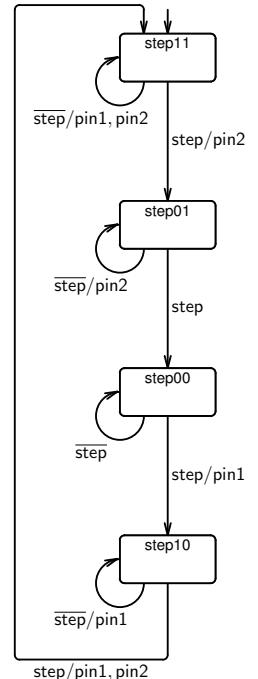
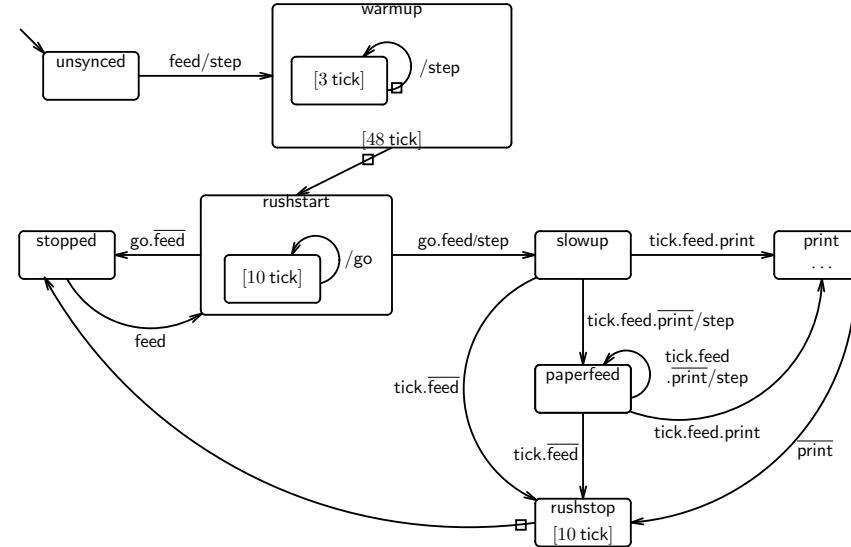
Reasoning about Stateflow designs is complicated:

1. intricate ordering rules
2. queued event processing
3. stacking of communications
4. implicit assumption of synchrony

Synchronous languages have *better* underlying models
(assumption)

An Argos [Mar91, MR01] block: syncblock [BS05]

- Our first attempt at combining synchronous languages and Simulink.
- Simulate with Argos controllers.



aside: [CCM⁺03, SSC⁺04]

- *integrate rather than extract*
- *simulate sync. programs*

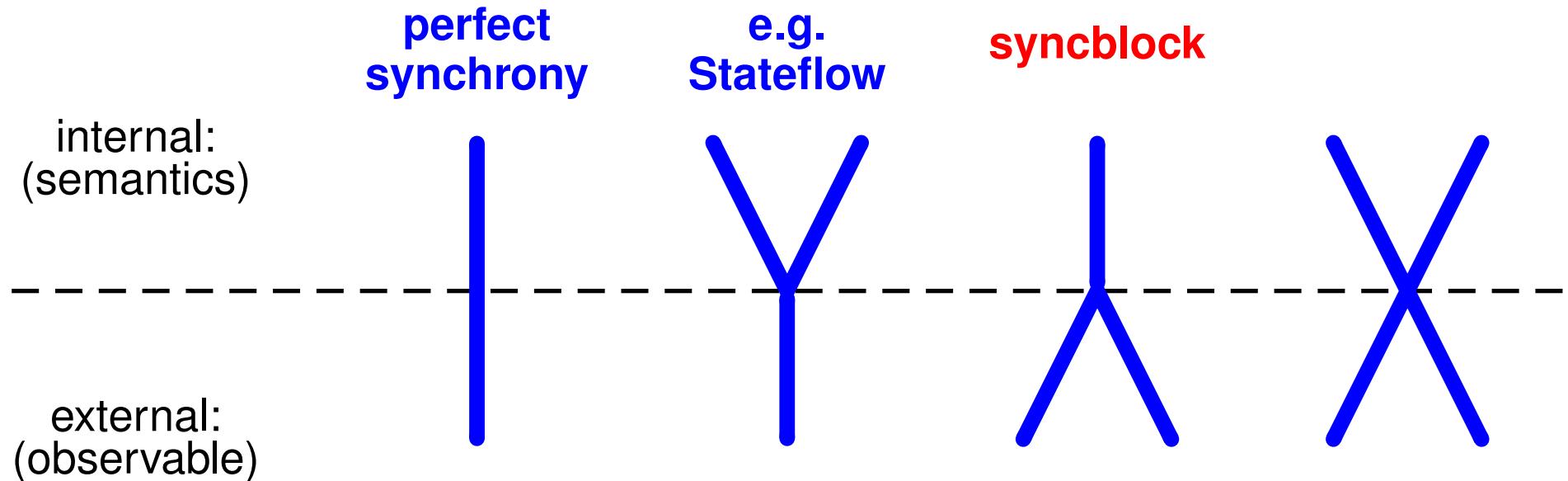
syncblock: simulating embedded controllers

- **Original Prototype:** perfect synchrony
 - Block outputs appear simultaneously with inputs.
 - i.e. in the same Simulink step.
- *But*, Simulink normally models timing detail.

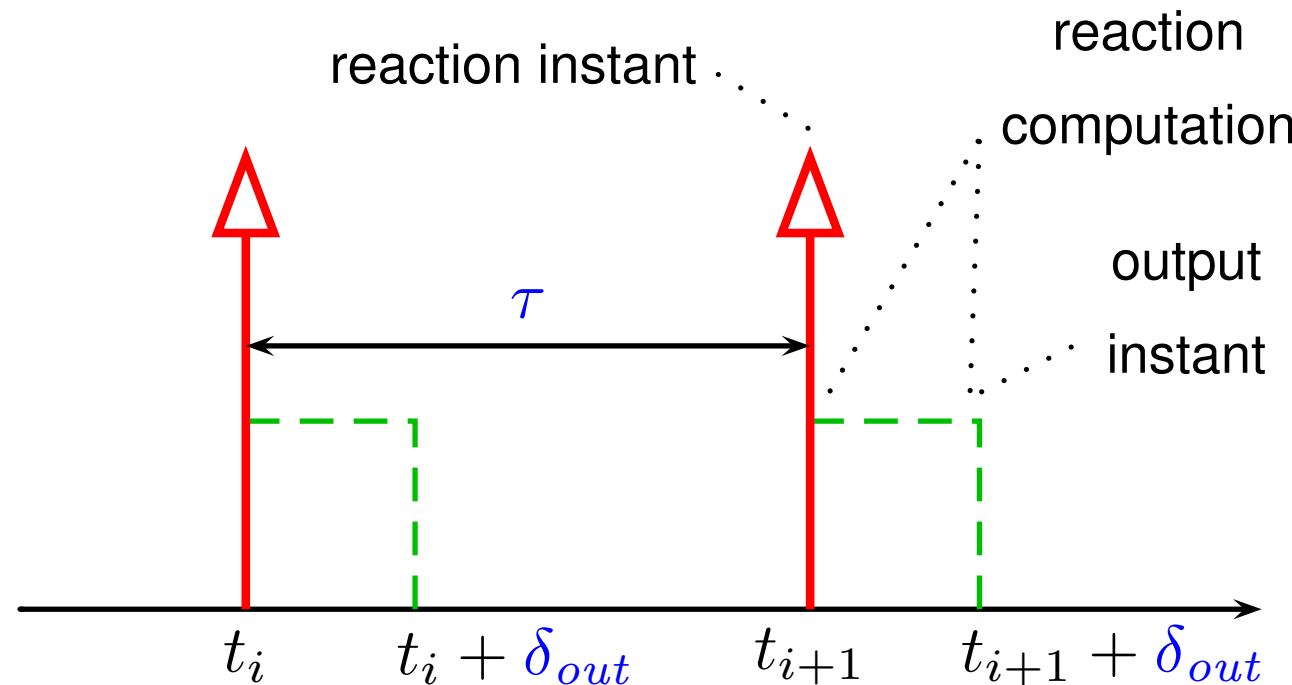
consider: dedicated embedded controllers

aim: provide simulation runs with low-level timing detail.

syncblock: simulating synchrony



- **Revised approach:** simulate implementation delays.
 - Internally: synchronous semantics.
 - Externally: delay between inputs and outputs.
- Necessary to **latch** inputs and outputs, and to **schedule** reactions.
 - Effectively modelling part of the platform (if abstractly).



Idealised parameters

- event-driven or sample-driven: mode **aside:** TAXYS [STY03]
 - Delay between input and output: δ_{out}
 - Minimum pause between reactions: τ
 - Program + Limitations = Simulation (block)
= Implementation (model)

Outline

✓ Simulink and Stateflow

✓ An Argos block

⇒ **Timing Model**

Embedding within Simulink

Concluding remarks

Transformation to Timed Automata

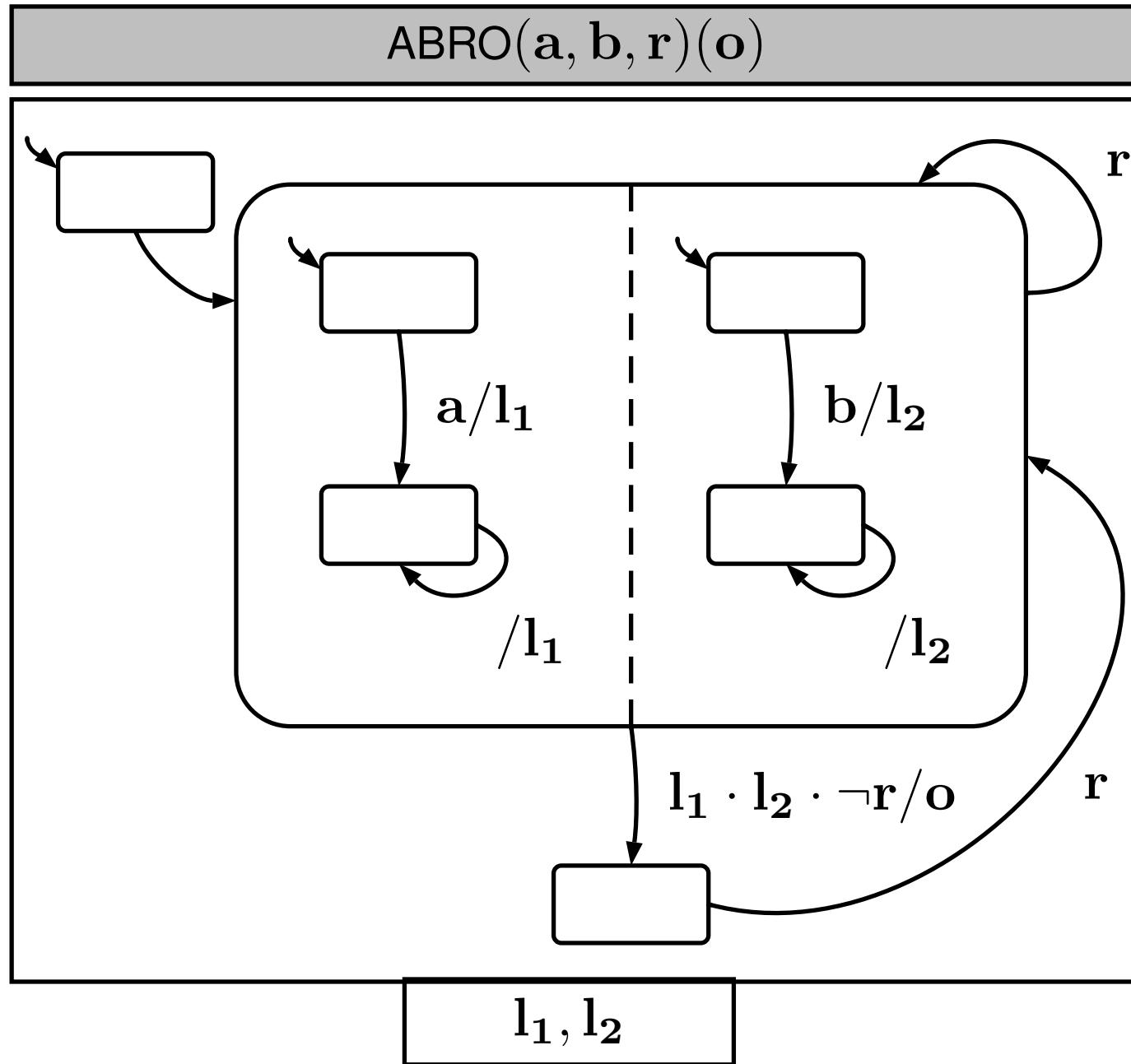
fix: $A_B = \langle S, s_0, I, O, T \rangle$ $\tau \in \mathbb{Q}_0^+$
 $trigger \in \{sample, event\}$ $\delta_{out} \in \mathbb{Q}_0^+$

requiring: $\delta_{out} \leq \tau$ $trigger = event \vee \tau > 0$

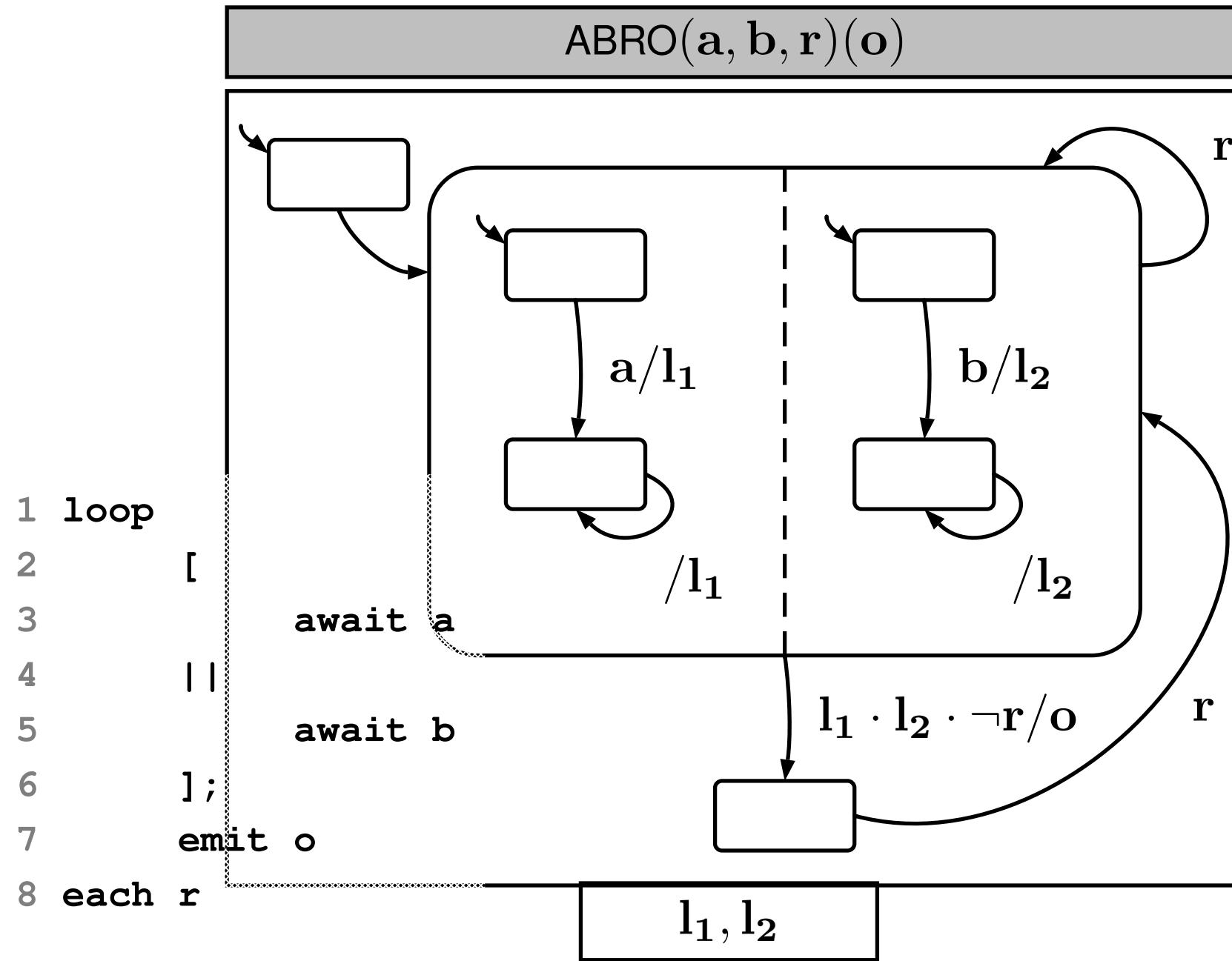
then define: $A_{\tau, \delta_{out}}^{trigger} = \langle \Sigma, L, L_0, C, E \rangle$: [AD94]

- $\Sigma = I \dot{\cup} O \dot{\cup} \{\text{react}\}$
- $L = (S \dot{\cup} \{\text{startup}\}) \times \mathcal{P}(I) \times \mathcal{P}(O) \times \mathbb{B}$
- $L_0 = \{(\text{startup}, \emptyset, \emptyset, \text{ff})\}$
- $C = \{x\}$
- E is the smallest set defined by the conjunction of 9 transition rules.

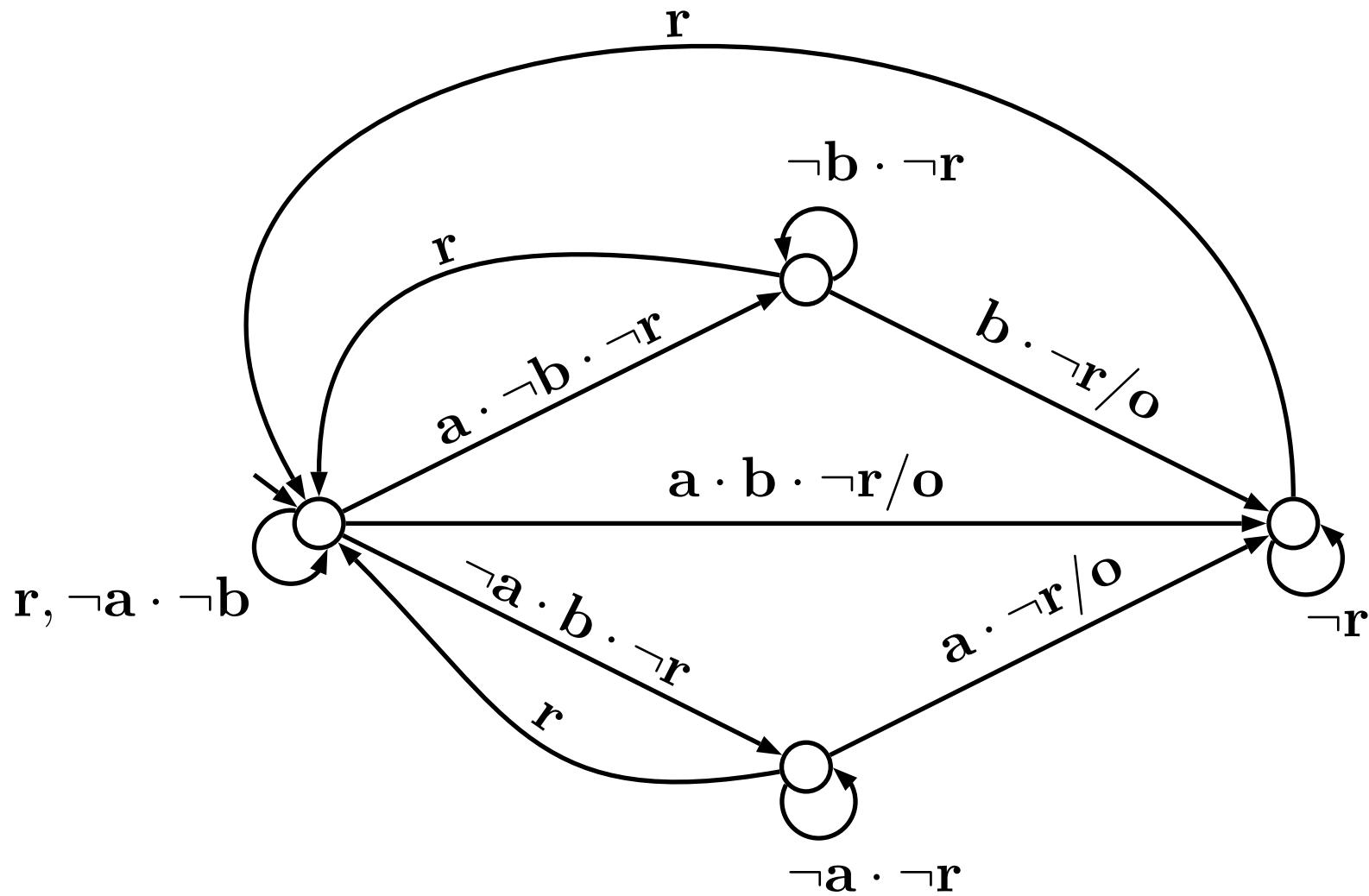
(almost) ABRO [Ber00]: in Argos



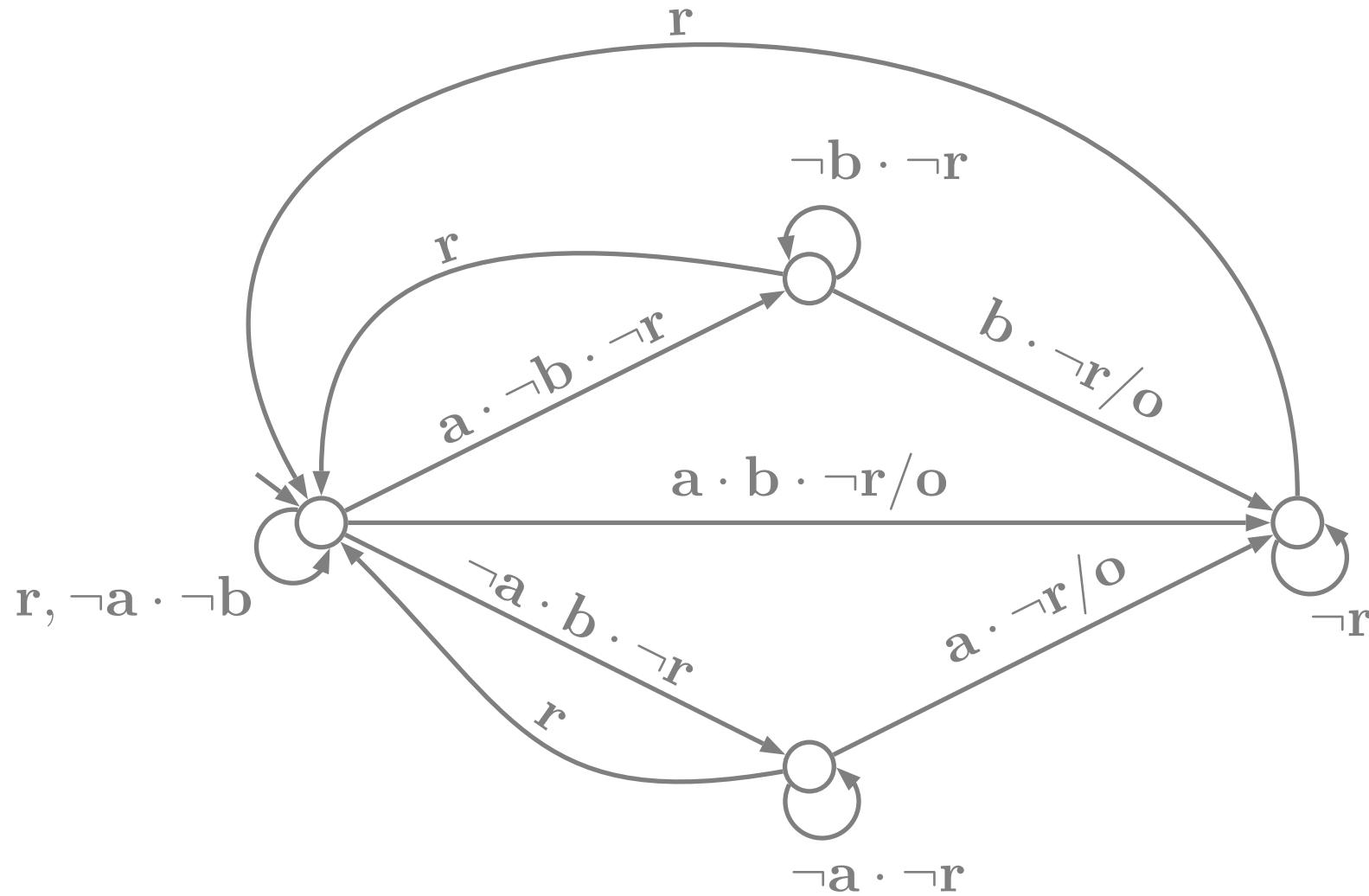
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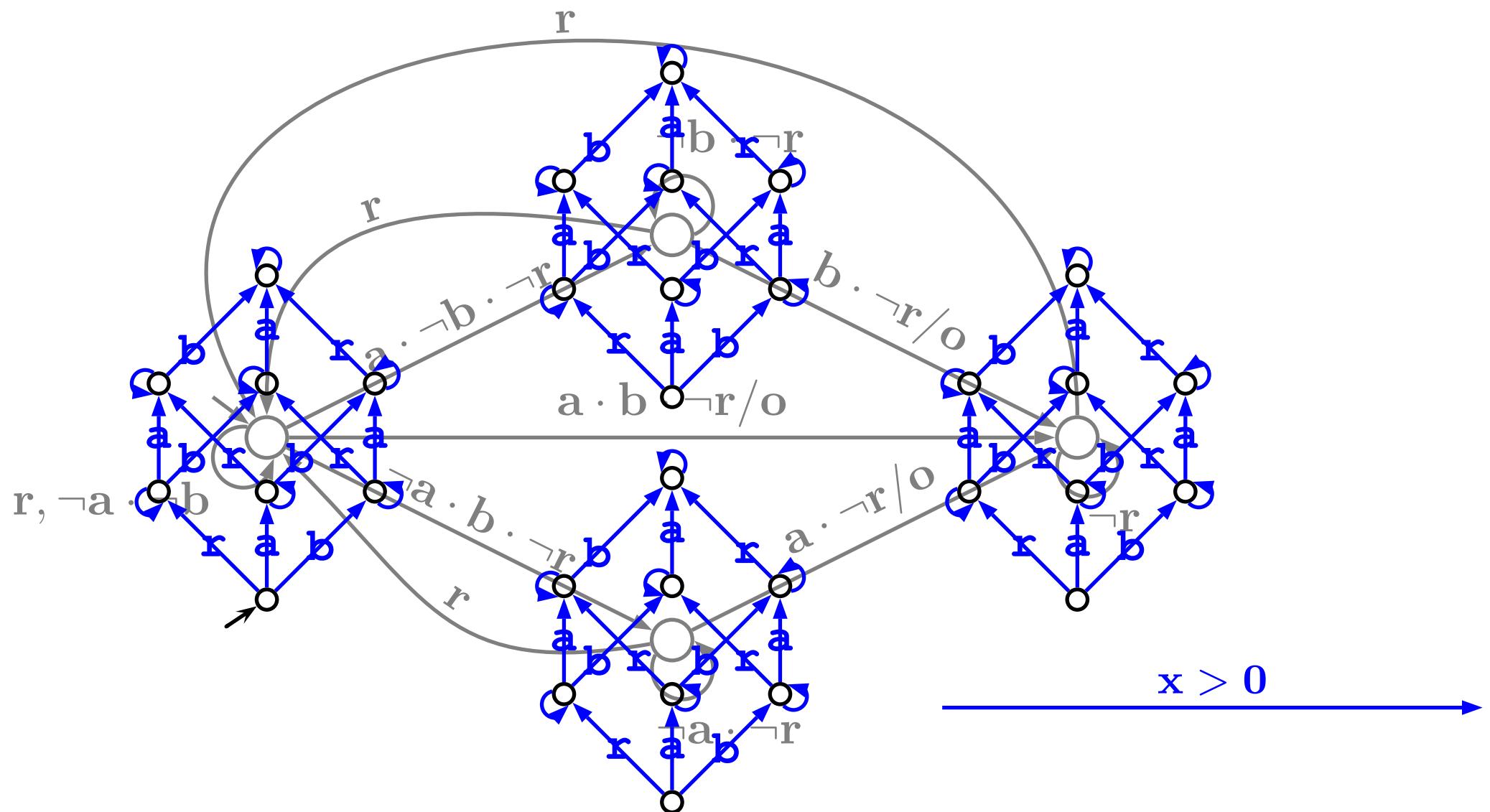
(almost) ABRO: Labelled Transition System



(almost) ABRO: Timed Transition System

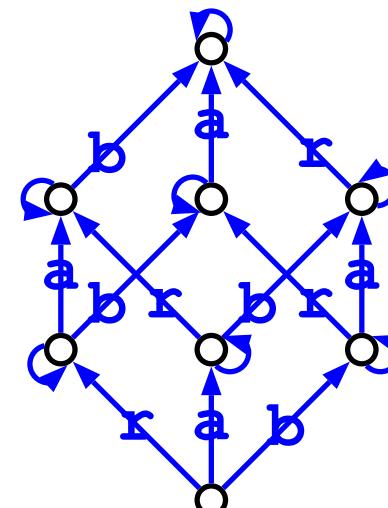
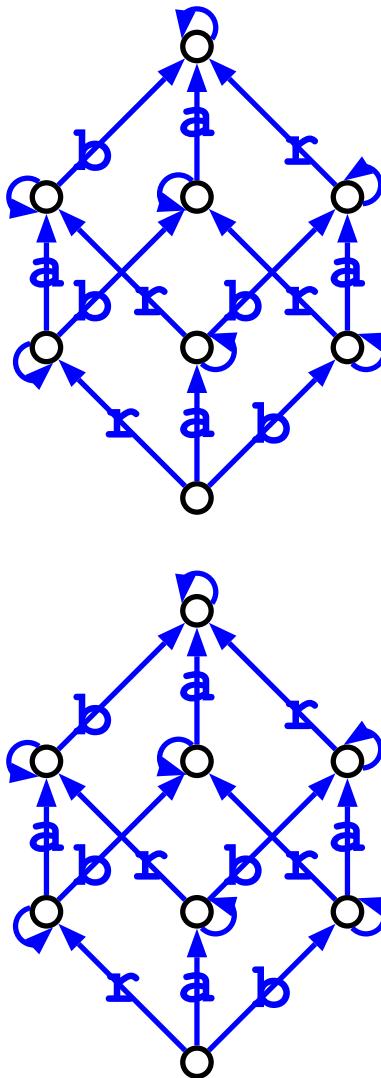
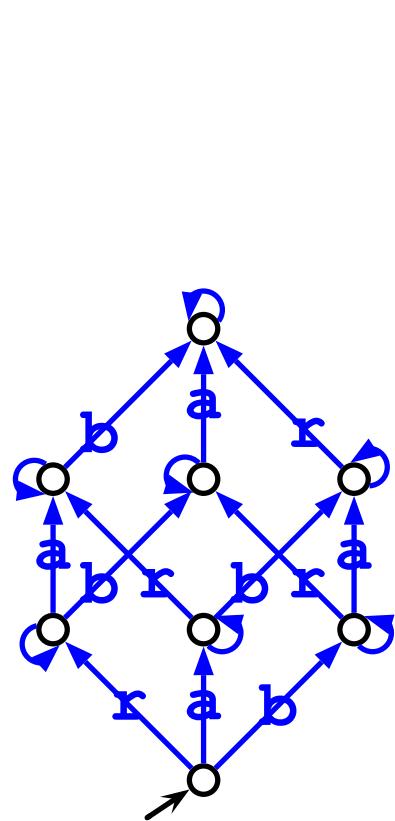


(almost) ABRO: Timed Transition System



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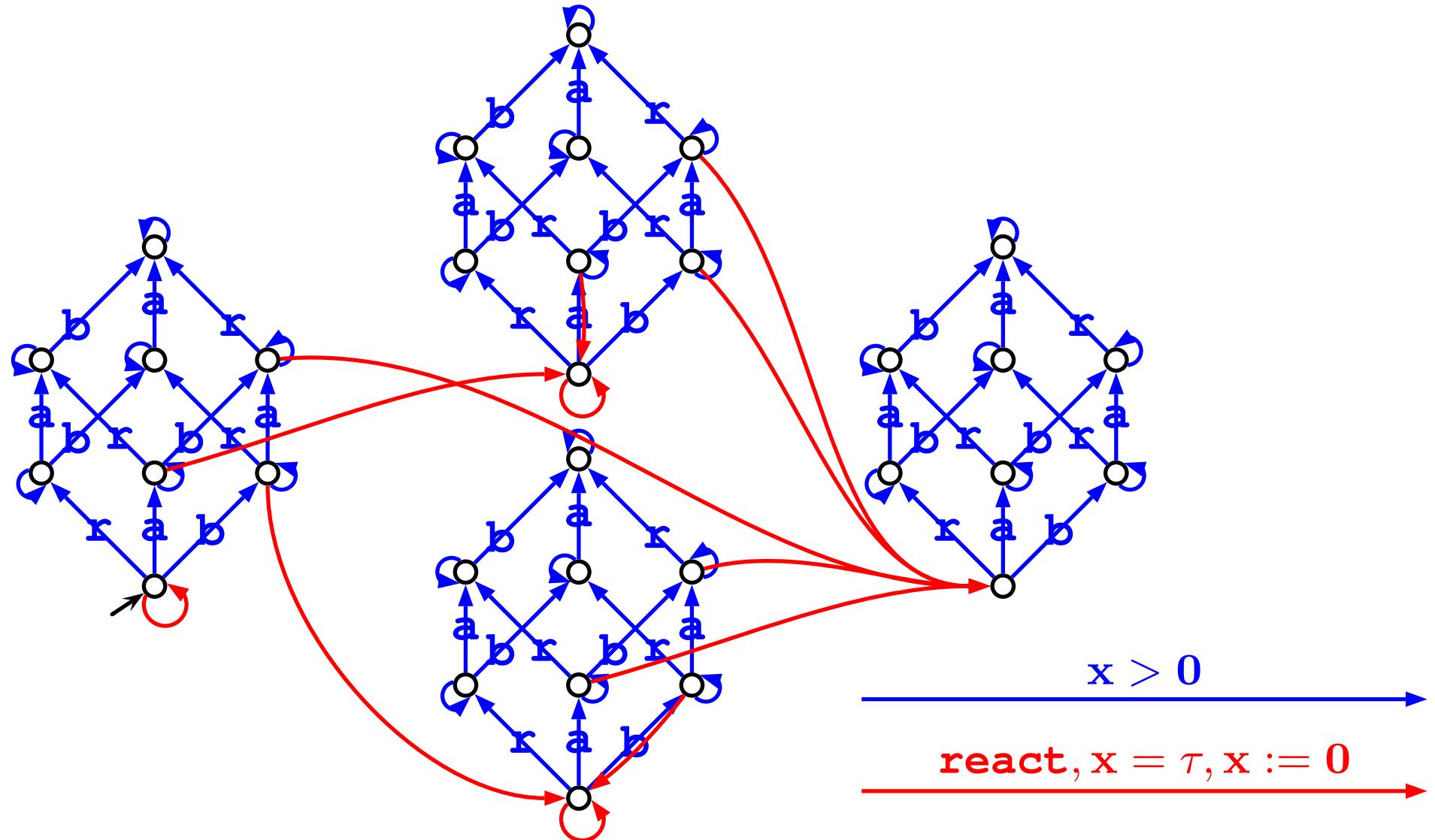
trigger = sample



$x > 0$

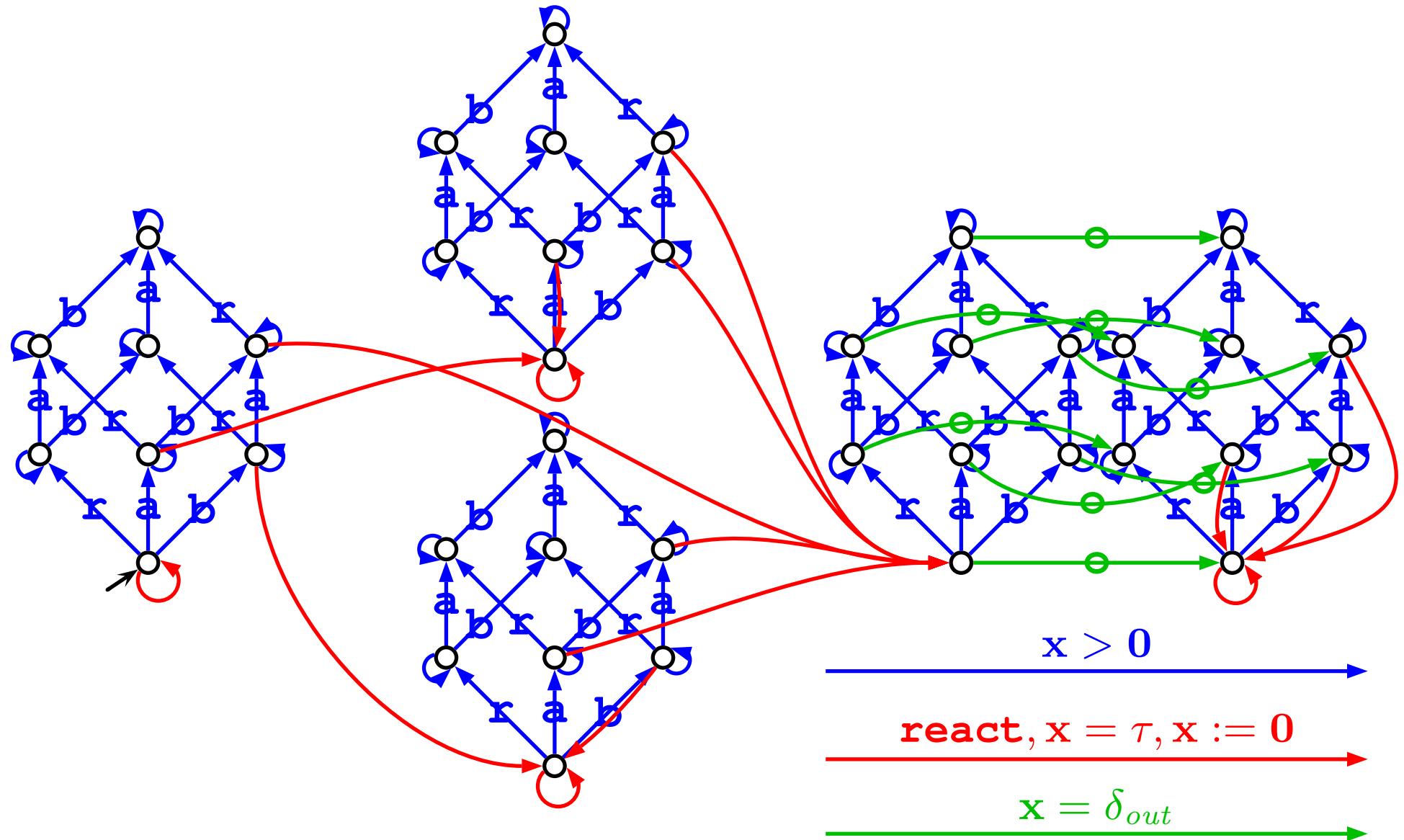
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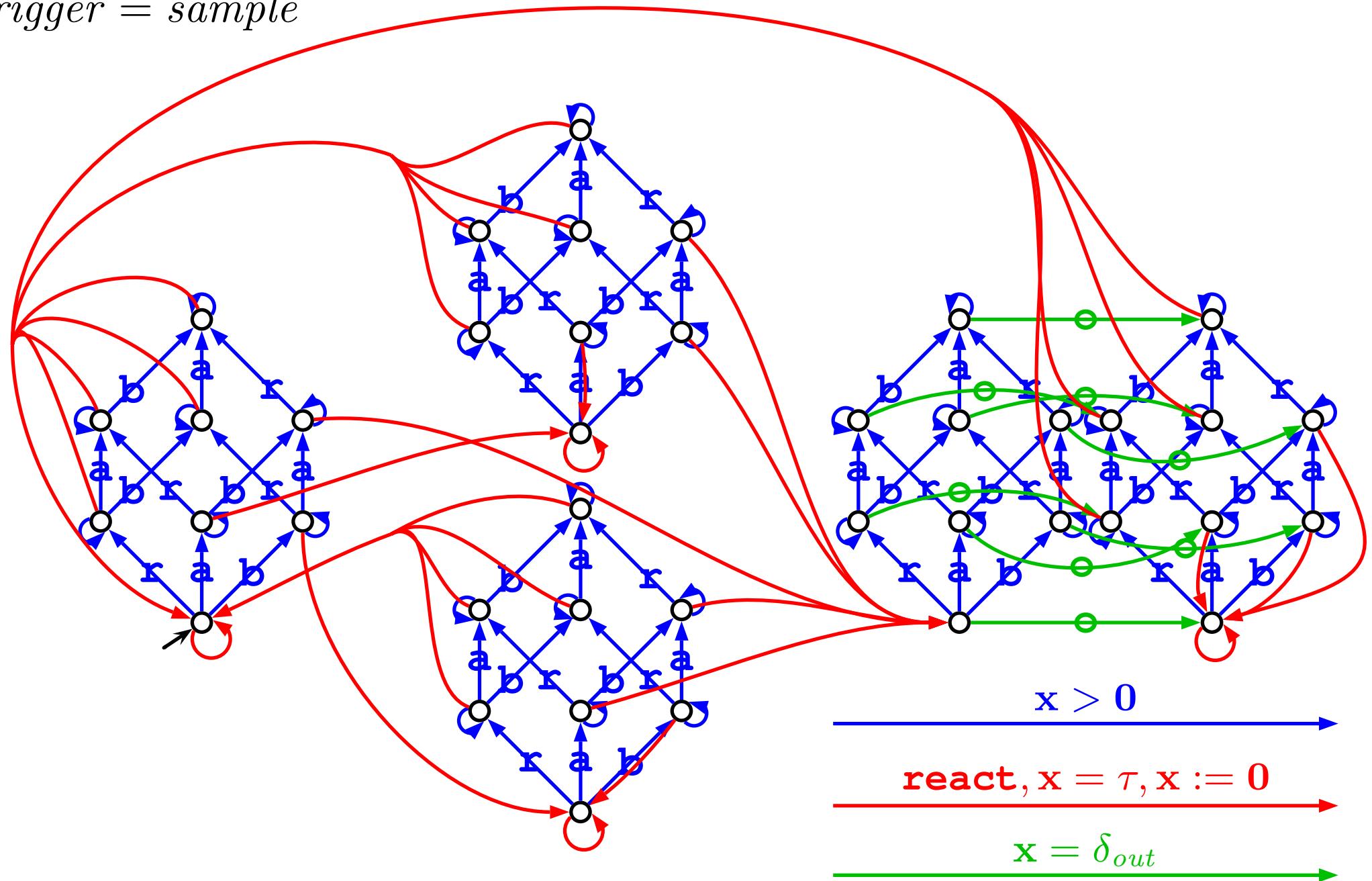
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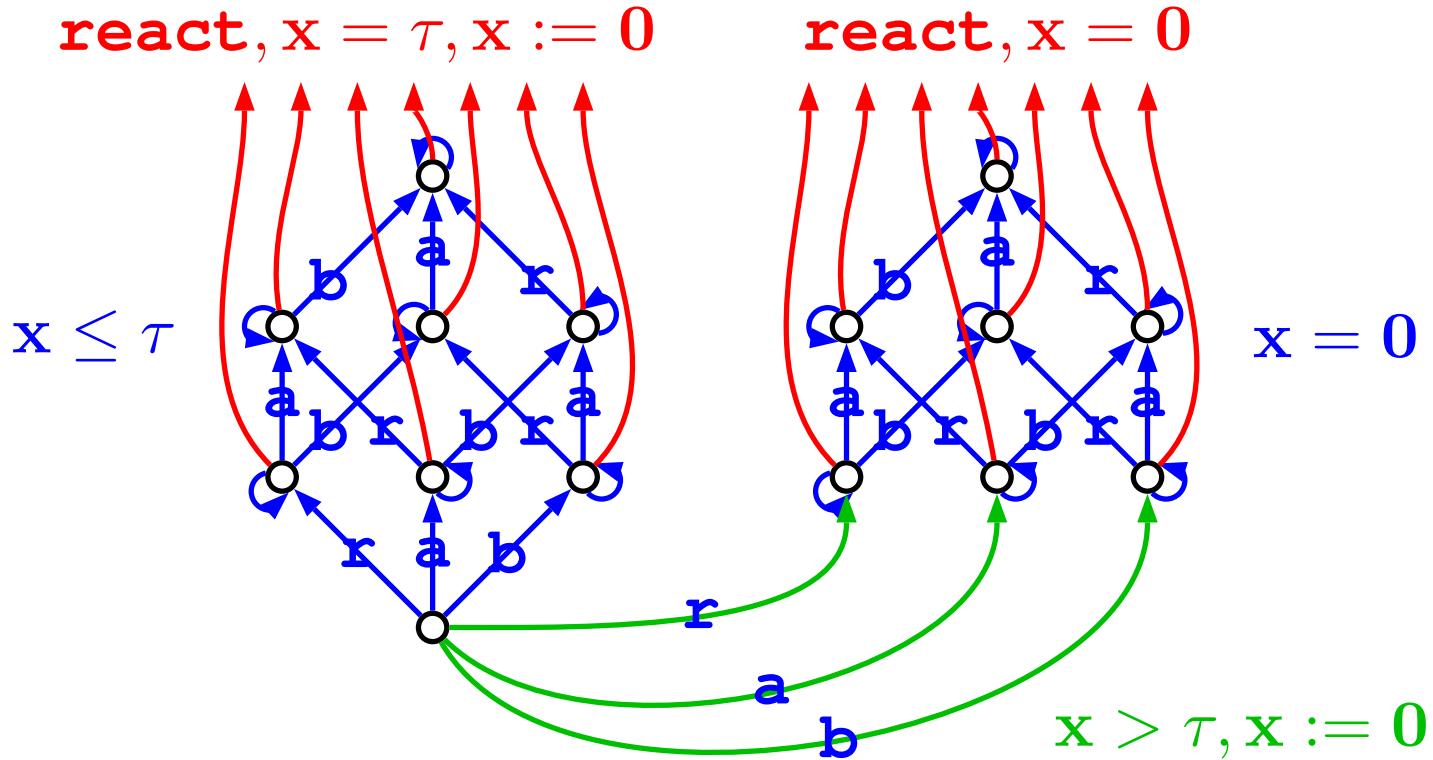
(almost) ABRO: Timed Transition System

trigger = sample



Event-driven triggering

trigger = event



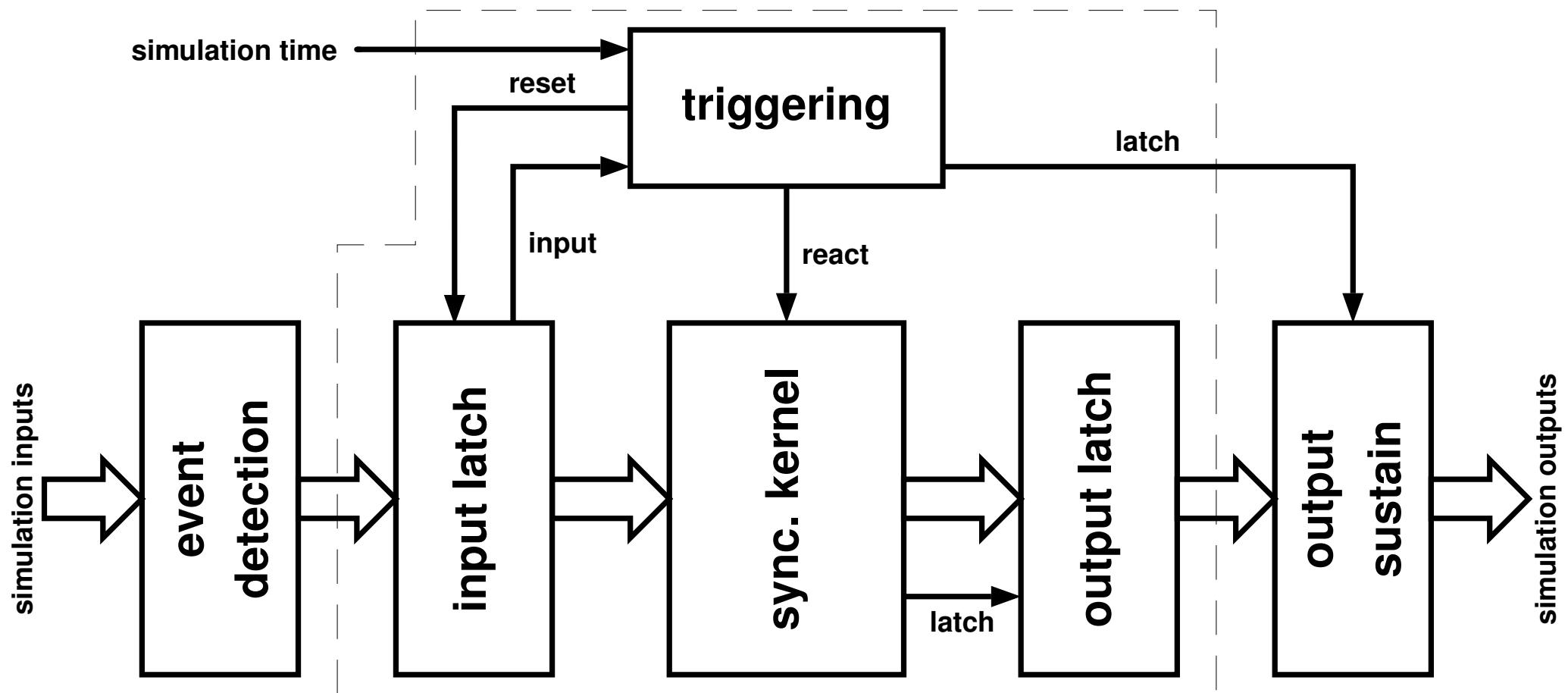
- Input events during a reaction must wait until $x = \tau$
- Otherwise, they trigger a reaction *urgently* [BST97]

Outline

- ✓ Simulink and Stateflow
 - ✓ An Argos block
 - ✓ Timing Model
- ⇒ Embedding within Simulink

Concluding remarks

Embedding within Simulink



One block or many?

Embedding within Simulink

Adopt a semantics for Simulink

- Simulation Engine
- Intent of models

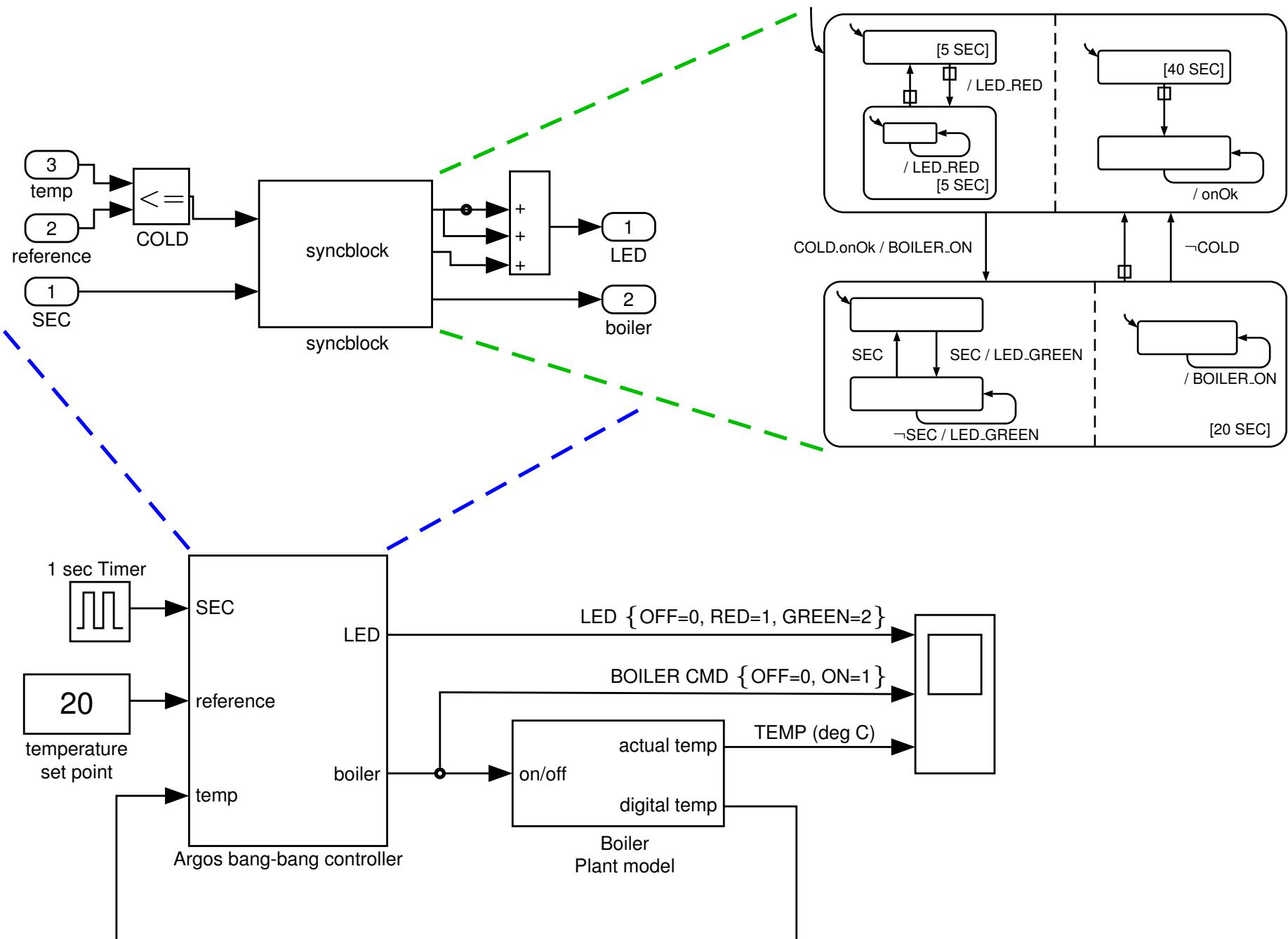
Translate models

e.g. to Lustre

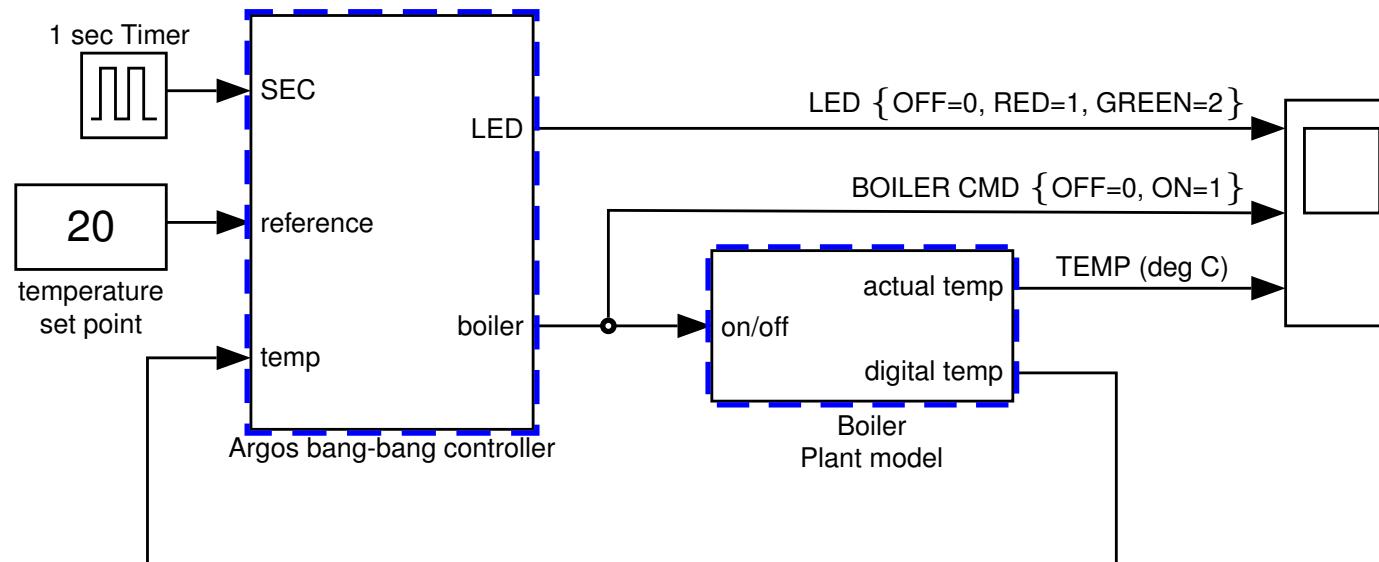
Interactions of block

mix conceptual and low-level operations

Mathworks Bang-bang temperature controller

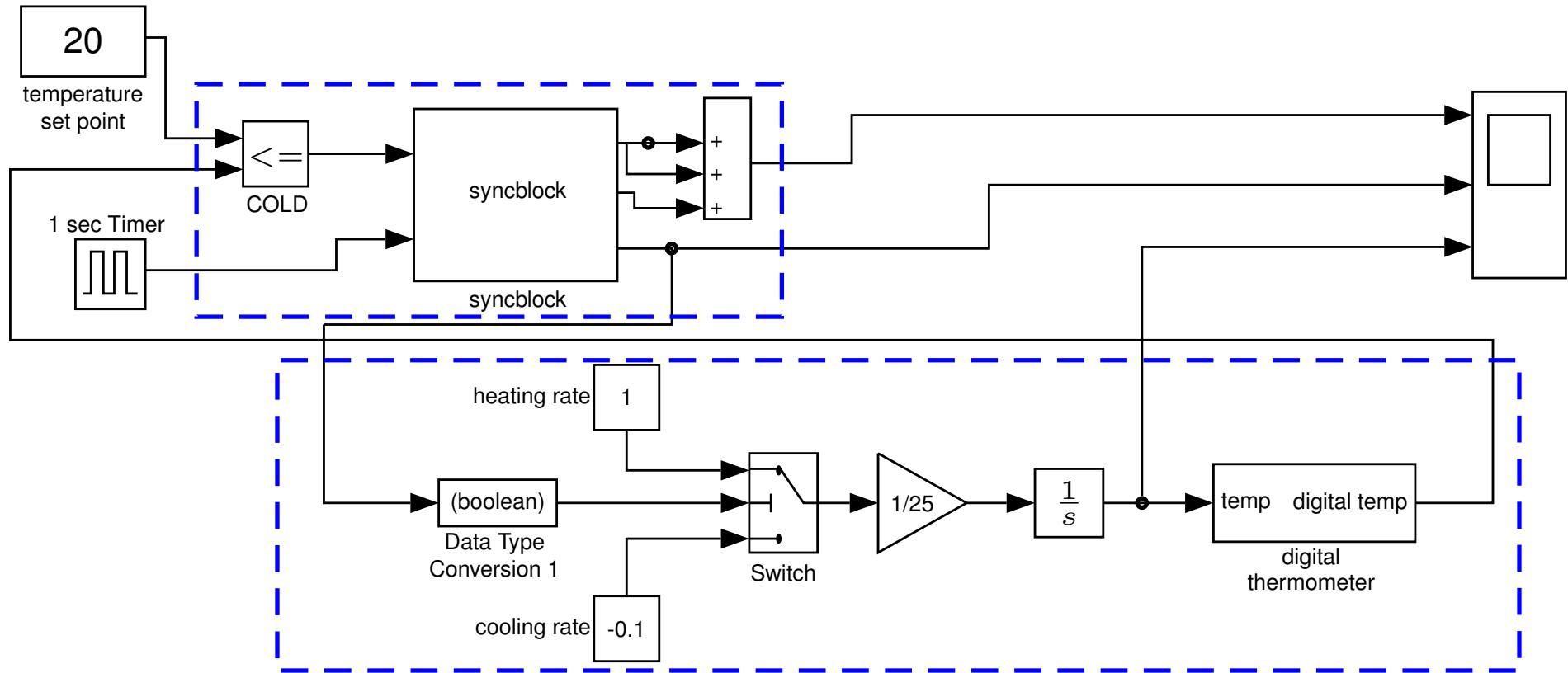


Simulink simulation engine: initialization



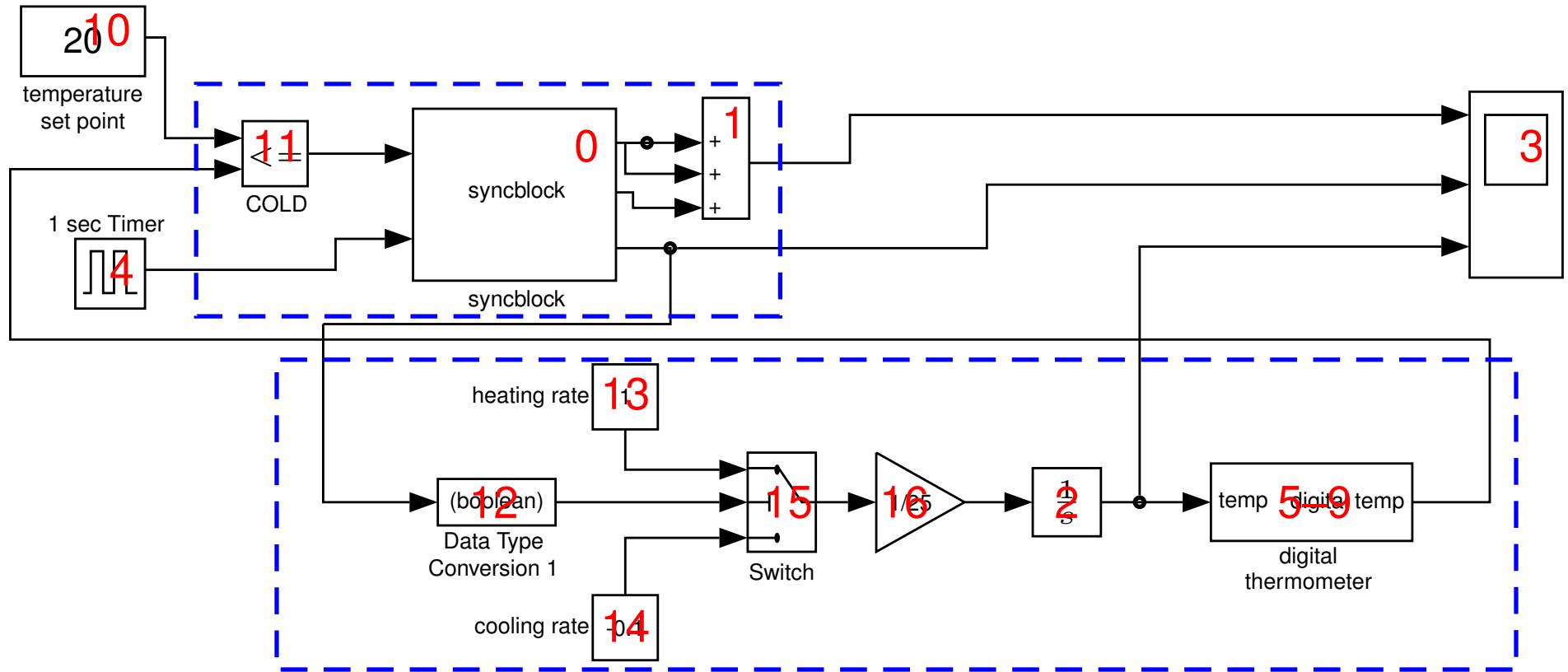
1. Flatten model

Simulink simulation engine: initialization



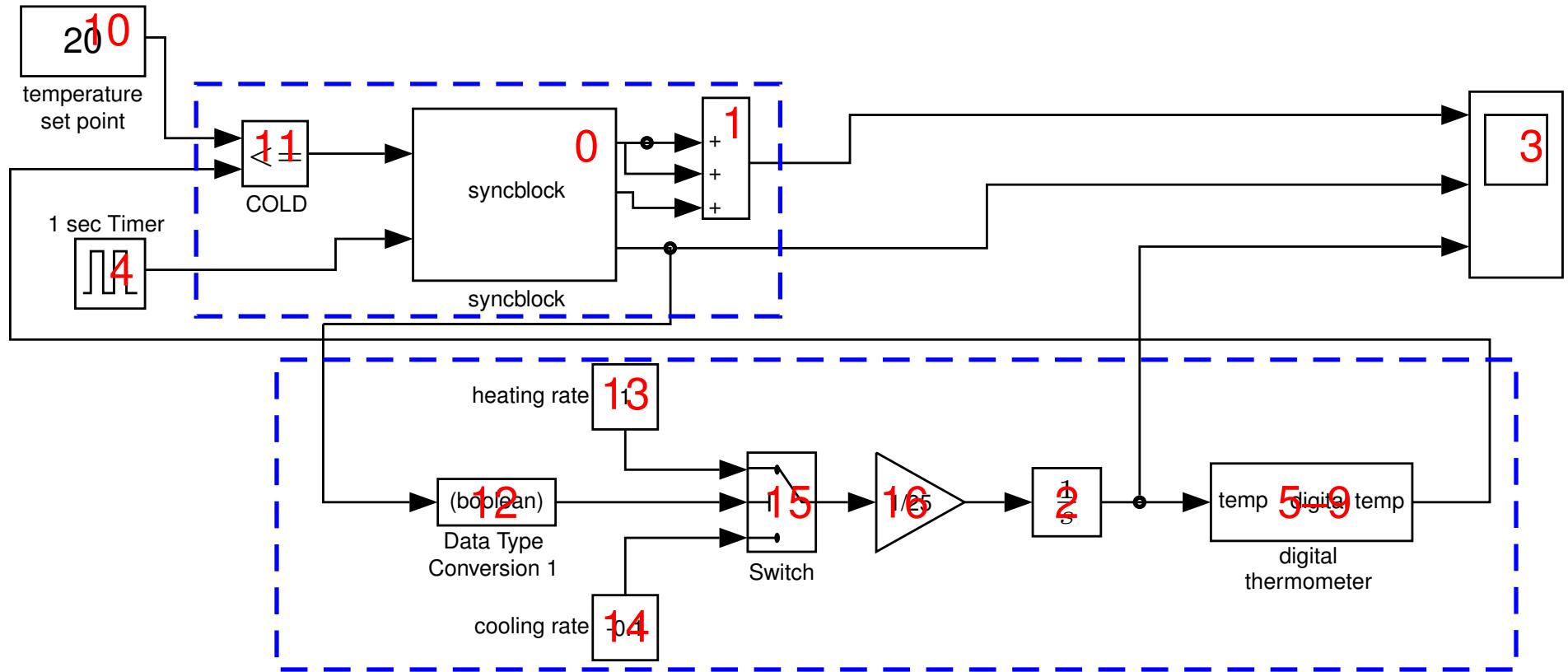
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Simulink simulation engine: initialization



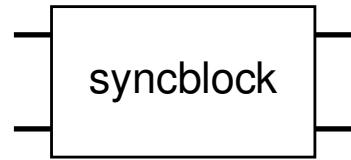
1. Flatten model
2. Order by signal dependencies.

Simulink simulation engine: initialization



1. Flatten model
2. Order by signal dependencies.
3. Start at $t = 0$.
4. Initialize all blocks.
5. Visit each block—maybe several times.
6. Increase t —depends on solver.
7. repeat from step 5

Behaviour of syncblock



$$\begin{aligned} y &= f_o(t, x, u) && \text{outputs} \\ x'_d &= f_u(t, x, u) && \text{update} \end{aligned}$$

x_c previous clock value

x_{t_p} previous sample time

- Two predicates: *react* and *emit*.
- Instants of interest:

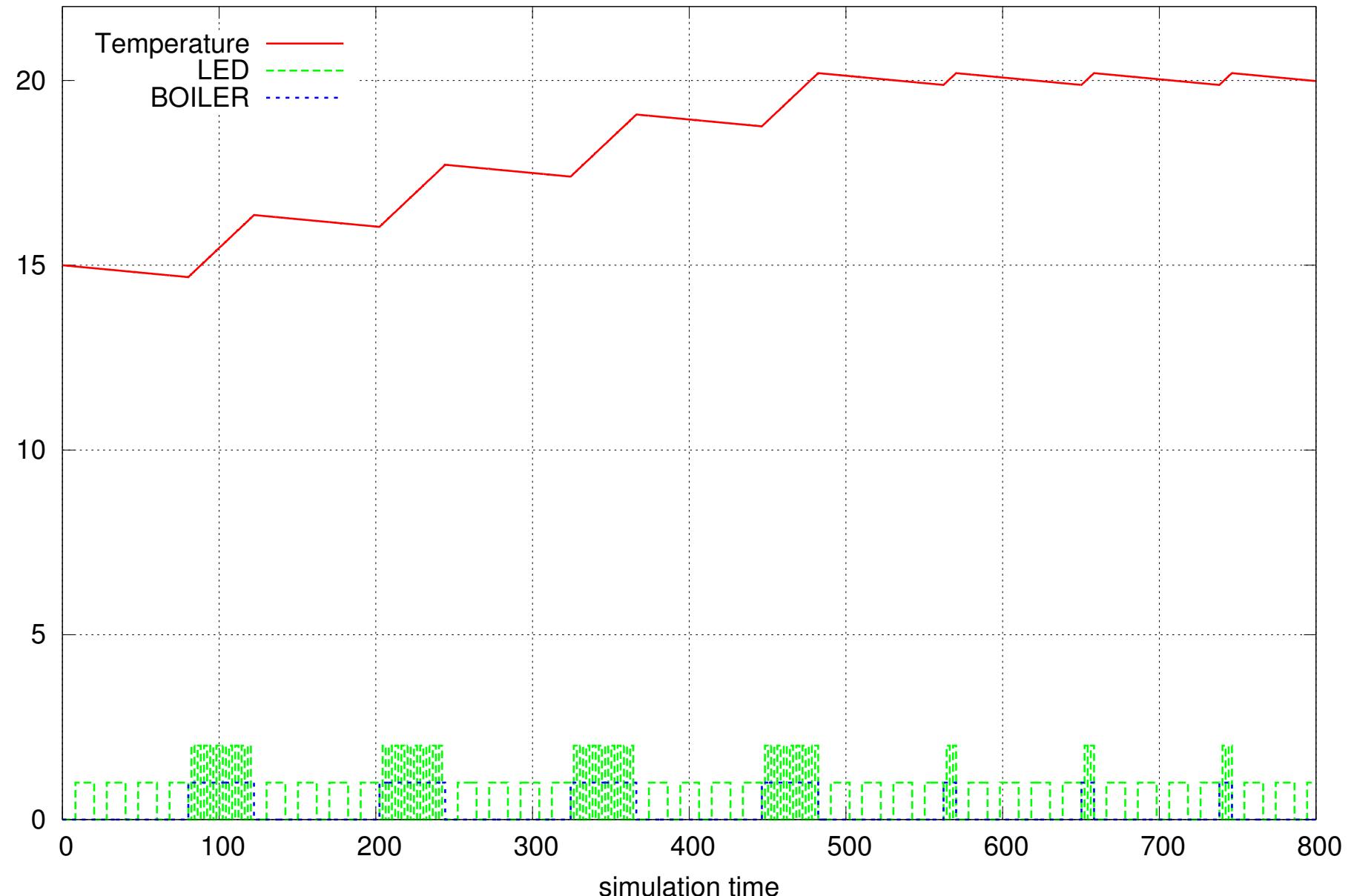
– sample-driven:

| | |
|-----------------------|--|
| $\delta_{out} = \tau$ | $[\tau, 0]$ |
| otherwise | $[\tau, 0]$ and $[\tau, \delta_{out}]$ |
| $\tau = 0$ | inherited |
| otherwise | zero-crossings |

– event-driven:

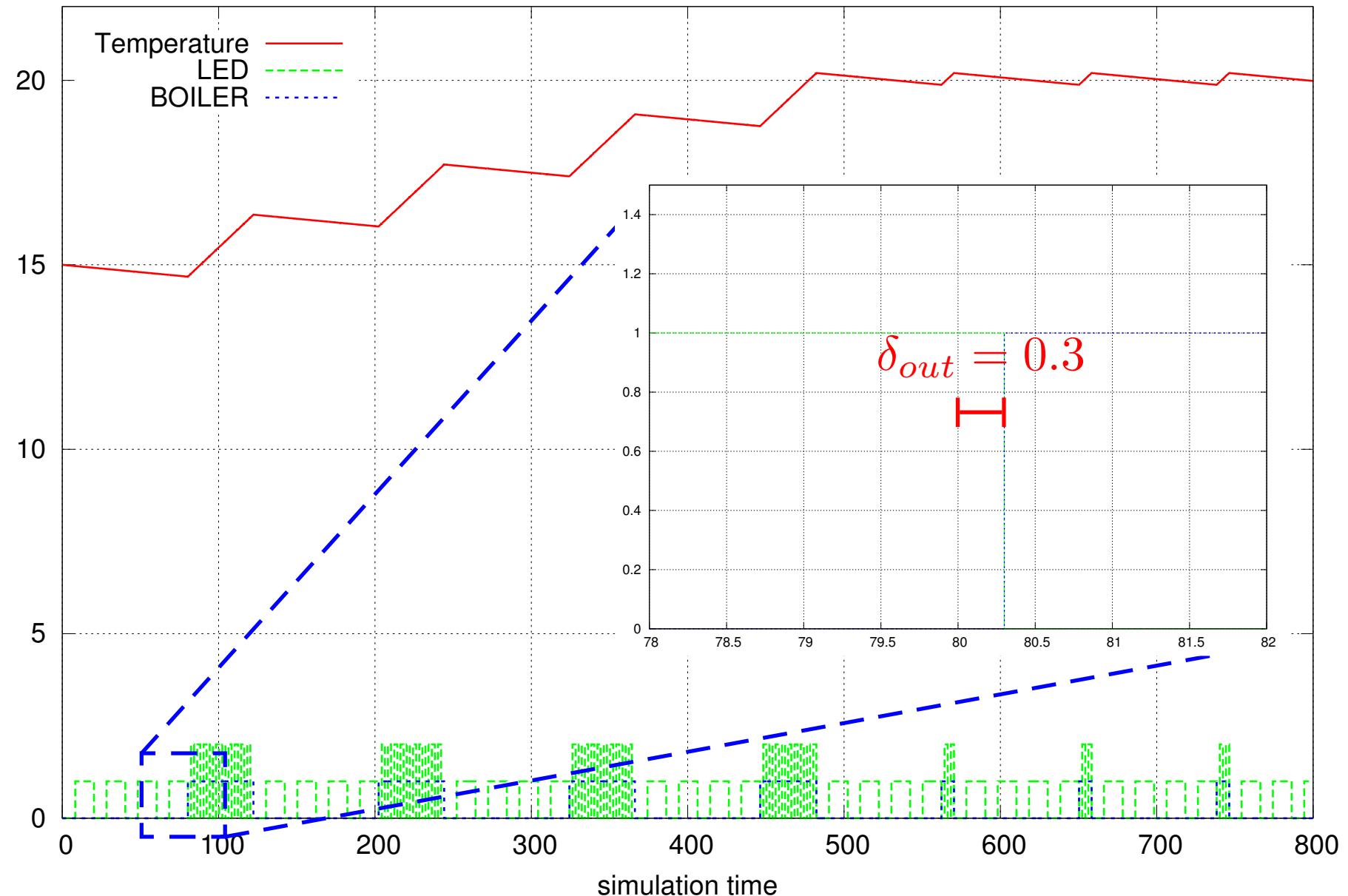
Effect of parameters

Bang-bang Controller: Stateflow



Effect of parameters

Bang-bang Controller: Stateflow



Summary

- ✓ Simulink and Stateflow
- ✓ An Argos block
- ✓ Timing Model
- ✓ Embedding within Simulink

⇒ Concluding remarks

- Working prototype uses Argos.
- Timed automata framework clarifies implementation.
- Looking for case-studies to evaluate utility.

Concluding remarks

References

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